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ICM7217

4-Digit LED Display, Programmable Up/Down Counter

July 2001

Features

- **Four Decade, Presettable Up-Down Counter with Parallel Zero Detect**
- **Settable Register with Contents Continuously Compared to Counter**
- **Directly Drives Multiplexed 7 Segment Common Anode or Common Cathode LED Displays**
- **On-Board Multiplex Scan Oscillator**
- **Schmitt Trigger On Count Input**
- **TTL Compatible BCD I/O Port, Carry/Borrow, Equal, and Zero Outputs**
- **Display Blank Control for Lower Power Operation; Quiescent Power Dissipation <5mW**
- **All Terminals Fully Protected Against Static Discharge**
- **Single 5V Supply Operation**

Jameco Part Number 43801

Description

The ICM7217 is a four digit, presettable up/down counter with an onboard presettable register continuously compared to the counter. The ICM7217 is intended for use in hard-wired applications where thumbwheel switches are used for loading data, and simple SPDT switches are used for chip control.

This circuit provides multiplexed 7 segment LED display outputs, with common anode or common cathode configurations available. Digit and segment drivers are provided to directly drive displays of up to 0.8 inch character height (common anode) at a 25% duty cycle. The frequency of the onboard multiplex oscillator may be controlled with a single capacitor, or the oscillator may be allowed to free run. Leading zeros can be blanked. The data appearing at the 7 segment and BCD outputs is latched; the content of the counter is transferred into the latches under external control by means of the Store pin.

The ICM7217 (common anode) and ICM7217A (common cathode) versions are decade counters, providing a maximum count of 9999, while the ICM7217B (common anode) and ICM7217C (common cathode) are intended for timing purposes, providing a maximum count of 5959.

This circuit provides 3 main outputs; a CARRY/BORROW output, which allows for direct cascading of counters, a ZERO output, which indicates when the count is zero, and an EQUAL output, which indicates when the count is equal to the value contained in the register. Data is multiplexed to and from the device by means of a three-state BCD I/O port. The CARRY/BORROW, EQUAL, ZERO outputs, and the BCD port will each drive one standard TTL load.

To permit operation in noisy environments and to prevent multiple triggering with slowly changing inputs, the count input is provided with a Schmitt trigger.

Input frequency is guaranteed to 2MHz, although the device will typically run with f_{IN} as high as 5MHz. Counting and comparing (EQUAL output) will typically run 750kHz maximum.

Part Number Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	DISPLAY DRIVER TYPE	COUNT OPTION/ MAX COUNT	PKG. NO.
ICM7217AIPI	-25 to 85	28 Ld PDIP	Common Cathode	Decade/9999	E28.6
ICM7217CIPI	-25 to 85	28 Ld PDIP	Common Cathode	Timing/5959	E28.6
ICM7217IJI	-25 to 85	28 Ld CERDIP	Common Anode	Decade/9999	F28.6
ICM7217BIJI	-25 to 85	28 Ld CERDIP	Common Anode	Timing/5959	F28.6

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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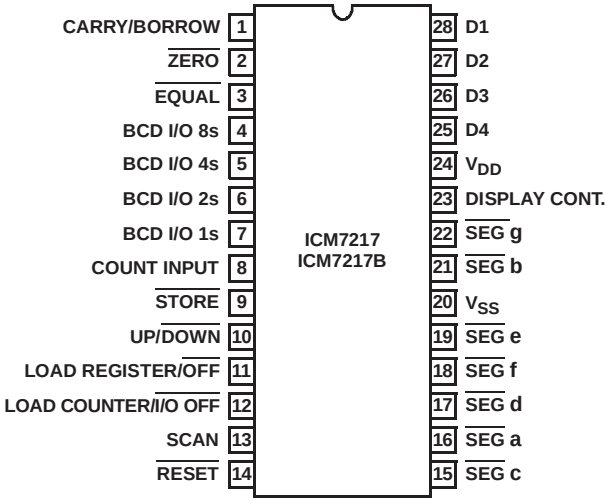
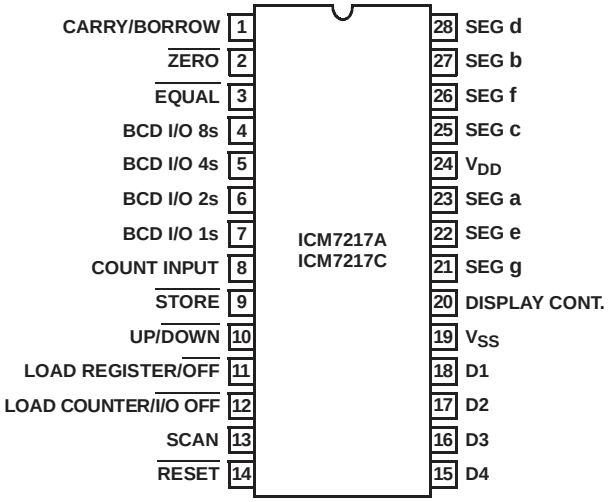
File Number **3167.3**

Pinouts

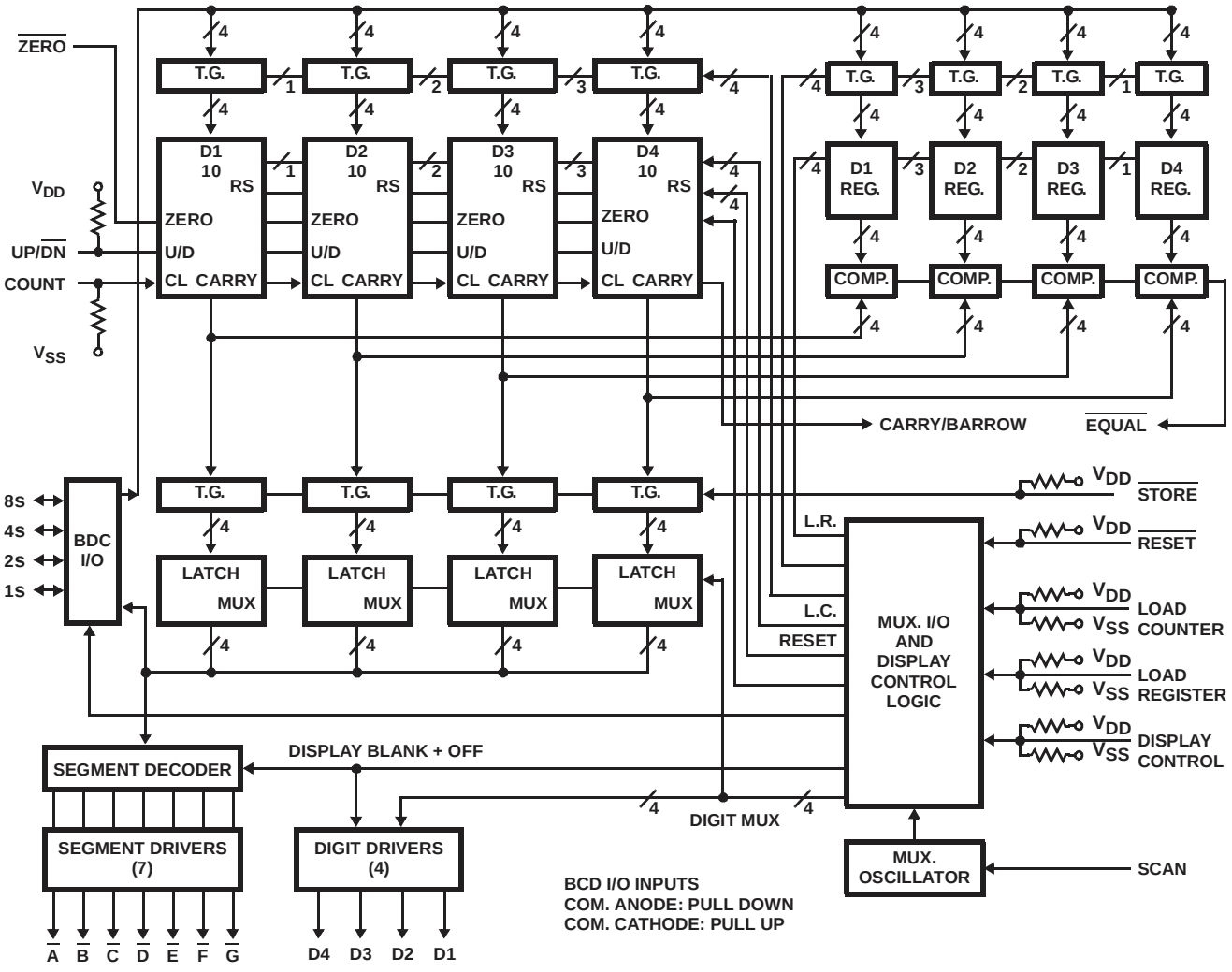
ICM7217 (CERDIP)
COMMON ANODE
TOP VIEW



ICM7217 (PDIP)
COMMON CATHODE
TOP VIEW



Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage (V_{DD} - V_{SS}) 6V
Input Voltage (Any Terminal) . . . . . (V_{SS} - 0.3V) to (V_{DD} + 0.3V) (Note 1)

Operating Conditions

Temperature Range . . . . . -25°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CERDIP Package	55	14
PDIP Package	55	N/A

Maximum Junction Temperature
PDIP Package . . . . . 150°C
CERDIP Package . . . . . 175°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering, 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason it is recommended that the power supply to the device be established before any inputs are applied and that in multiple systems the supply to the ICM7217 be turned on first.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{DD} = 5V, V_{SS} = 0V, T_A = 25°C, Display Diode Drop 1 .7V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current (Lowest Power Mode), IDD (7217)	Display Off, LC, DC, UP/DN, ST, RS, BCD I/O Floating or at V_{DD} (Note 1)	-	350	500	µA
Supply Current, OPERATING, I_{OP}	Common Anode, Display On, all "8's"	140	200	-	mA
Supply Current, OPERATING, I_{OP}	Common Cathode, Display On, all "8's"	50	100	-	mA
V_{SUPPLY}, V_{DD}		4.5	5	5.5	V
Digit Driver Output Current, I_{DIG}	Common Anode, V_{OUT} = V_{DD} - 2.0V	140	200	-	mA_{PEAK}
SEGment Driver Output Current, ISEG	Common Anode, V_{OUT} = +1.5V	20	35	-	mA_{PEAK}
Digit Driver, Output Current, I_{DIG}	Common Cathode, V_{OUT} = +1.0V	-50	-75	-	mA_{PEAK}
SEGment Driver Output Current, ISEG	Common Cathode V_{OUT} = V_{DD} - 2V	-9	-12.5	-	mA_{PEAK}
$\overline{ST}$, $\overline{RS}$, UP/$\overline{DN}$ Input Pullup Current, IP	V_{IN} = V_{DD} - 2V (Note 1)	5	25	-	µA
3 Level Input Impendance, ZIN		40	-	350	kΩ
BCD I/O Input, High Voltage VBIH	ICM7217 Common Anode (Note 2)	1.5	-	-	V
	ICM7217 Common Cathode (Note 2)	4.40	-	-	V
BCD I/O Input, Low Voltage VBIL	ICM7217 Common Anode (Note 2)	-	-	0.60	V
	ICM7217 Common Cathode (Note 2)	-	-	3.2V	V
BCD I/O Input, Pullup Current IBPU	ICM7217 Common Cathode V_{IN} = V_{DD} - 2V (Note 2)	5	25	-	µA
BCD I/O Input Pulldown Current, IBPD	ICM7217 Common Anode V_{IN} = +2V (Note 2)	5	25	-	µA
BCD I/O, $\overline{ZERO}$, $\overline{EQUAL}$ Outputs Output High Voltage, VOH	I_{OH} = -100µA	3.5	-	-	V
BCD I/O, CARRY/BORROW $\overline{ZERO}$, $\overline{EQUAL}$ Outputs Output Low Voltage, V_{OL}	I_{OL} = 1.6mA	-	-	0.4	V
Count Input Frequency, f_{IN}	-20°C to 70°C	-	5	-	MHz
	Guaranteed	0	-	2	MHz
Count Input Threshold, VTH	(Note 3)	-	2	-	V
Count Input Hysteresis, VHYS	(Note 3)	-	0.5	-	V
Count Input LO, VCIL		-	-	0.40	V
Count Input HI, VCIH		3.5	-	-	V

Electrical Specifications

V_{DD} = 5V, V_{SS} = 0V, T_A = 25^{o}C, Display Diode Drop 1 .7V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Display Scan Oscillator Frequency, f_{DS}	Free-running (SCAN Terminal Open Circuit)	-	2.5	10	kHz

Switching Specifications

V_{DD} = 5V, V_{SS} = 0V, T_A = 25^{o}C

PARAMETER	MIN	TYP	MAX	UNIT
UP/$\overline{\text{DOWN}}$ Setup Time, t_{UCS}	300	-	-	ns
UP/$\overline{\text{DOWN}}$ Hold Time, t_{UCH}	1500	750	-	ns
COUNT Pulse Width High, t_{CWH}	250	100	-	ns
COUNT Pulse Width Low, t_{CWI}	250	100	-	ns
COUNT to CARRY/BORROW Delay, t_{CB}	-	750	-	ns
CARRY/BORROW Pulse Width t_{BW}	-	100	-	ns
COUNT to $\overline{\text{EQUAL}}$ Delay, t_{CE}	-	500	-	ns
COUNT to $\overline{\text{ZERO}}$ Delay, t_{CZ}	-	300	-	ns
RESET Pulse Width, t_{RST}	1000	500	-	ns

NOTES:

1. In the ICM7217 the UP/$\overline{\text{DOWN}}$, $\overline{\text{STORE}}$, $\overline{\text{RESET}}$ and the BCD I/O as inputs have pullup or pulldown devices which consume power when connected to the opposite supply. Under these conditions, with the display off, the device will consume typically 750µA.
2. These voltages are adjusted to allow the use of thumbwheel switches for the ICM7217. Note that a high level is taken as an input logic zero for ICM7217 common-cathode versions.
3. Parameters not tested (Guaranteed by Design).

Timing Waveforms

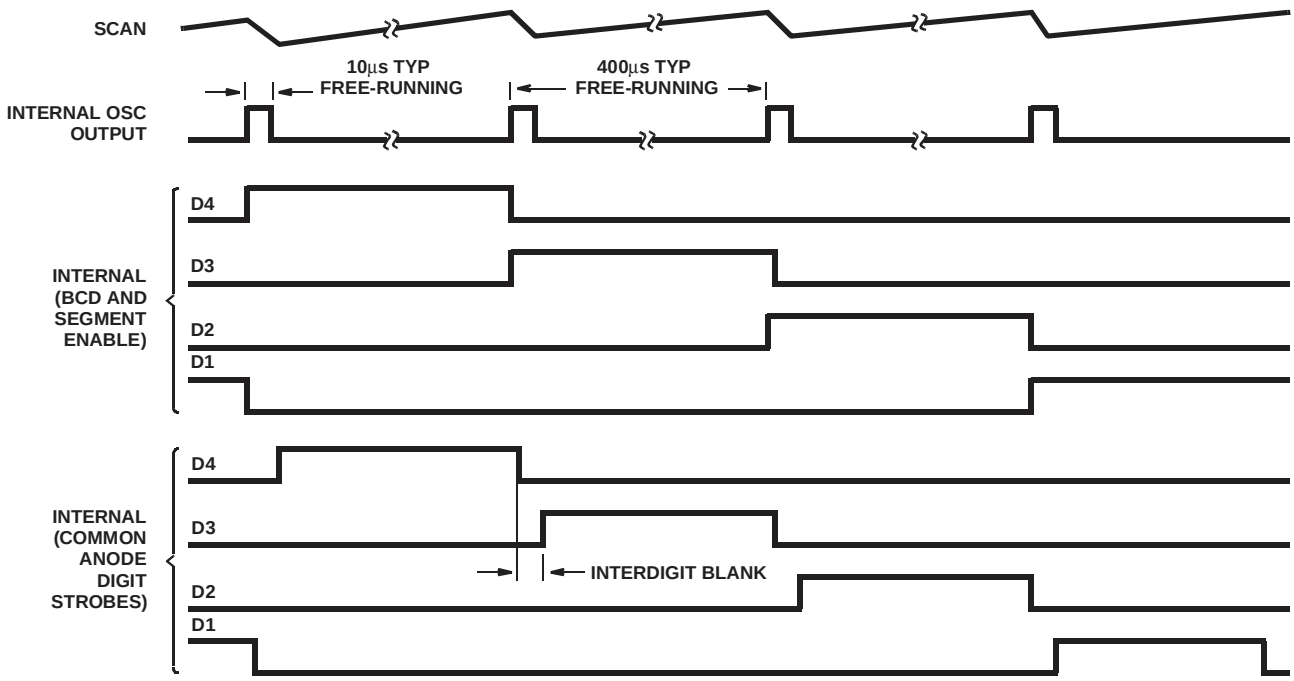


FIGURE 1. MULTIPLEX TIMING

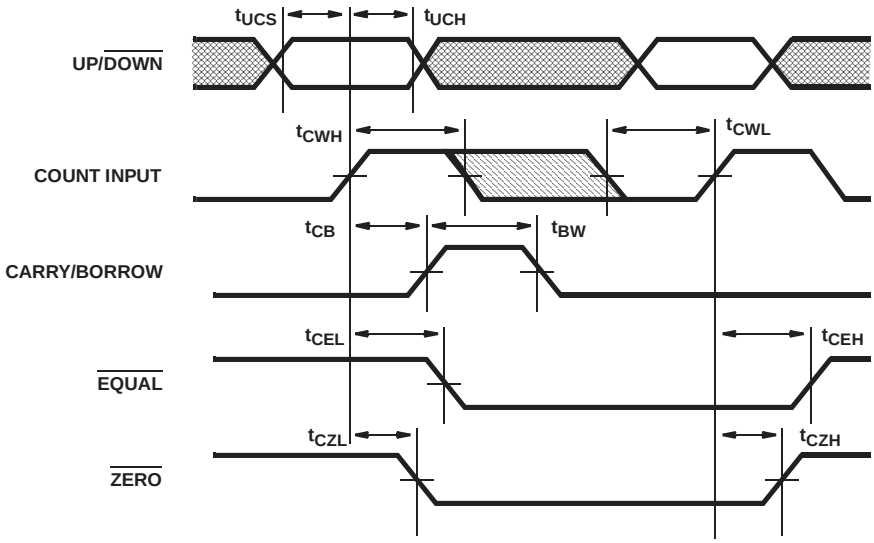


FIGURE 2. COUNT AND OUTPUTS TIMING

Timing Waveforms

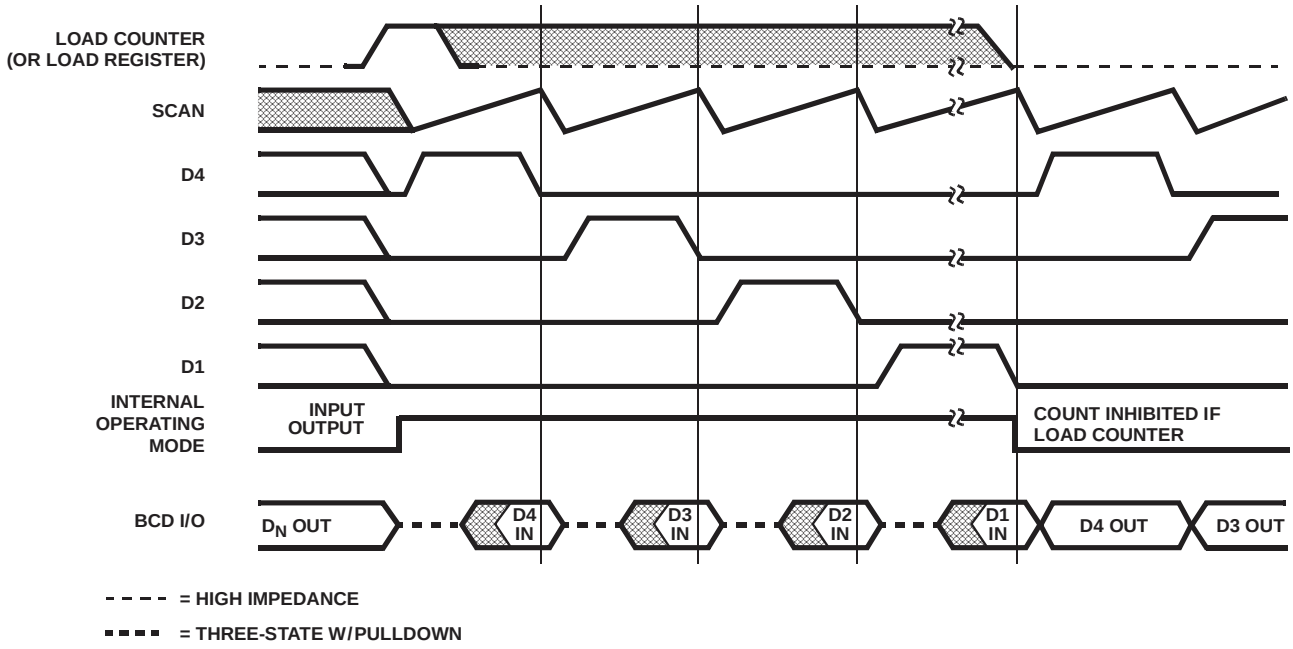


FIGURE 3. BCD I/O AND LOADING TIMING

Typical Performance Curves

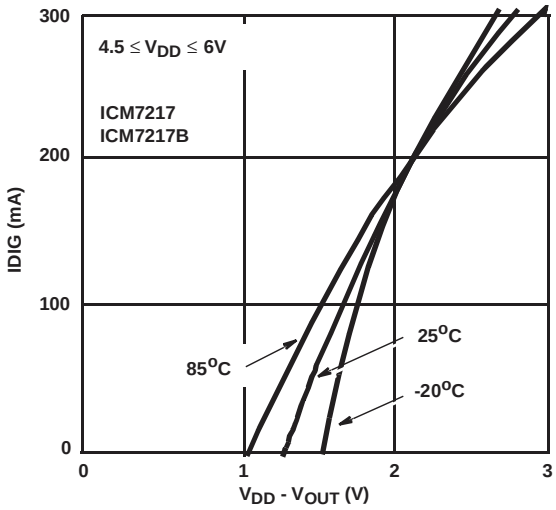


FIGURE 4. TYPICAL IDIG vs V+

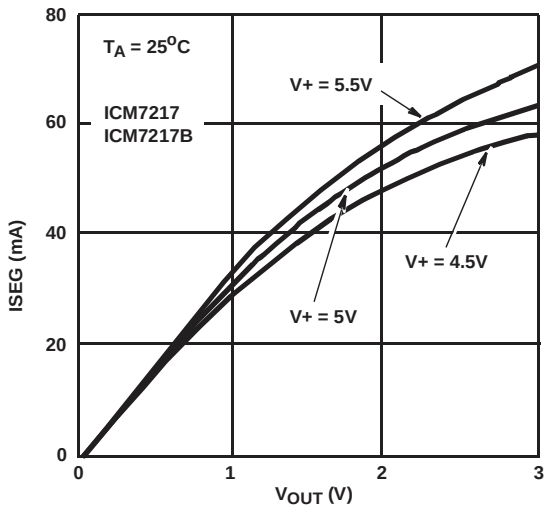


FIGURE 5. TYPICAL ISEG vs V_{OUT}

Typical Performance Curves

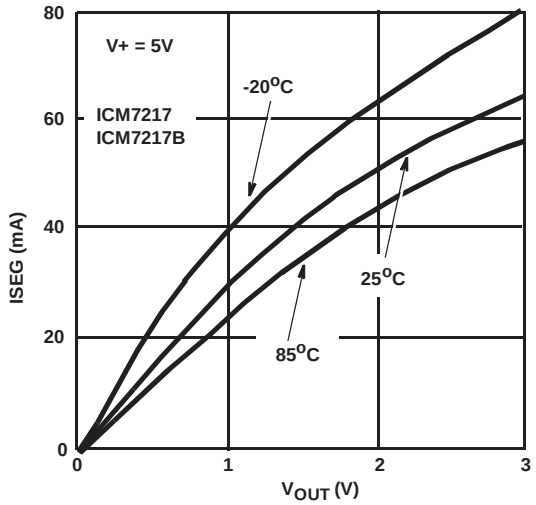


FIGURE 6. TYPICAL ISEG vs V_{OUT}

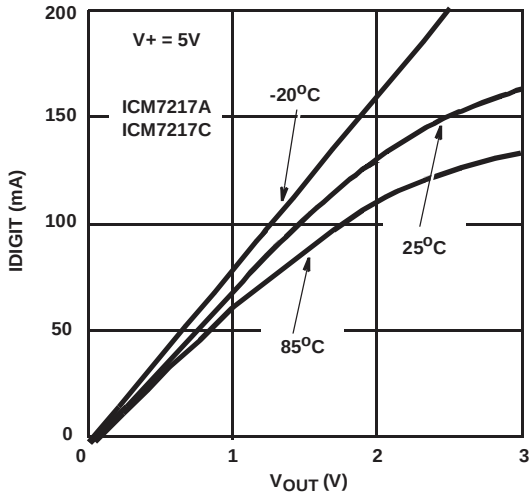


FIGURE 7. TYPICAL IDIGIT vs V_{OUT}

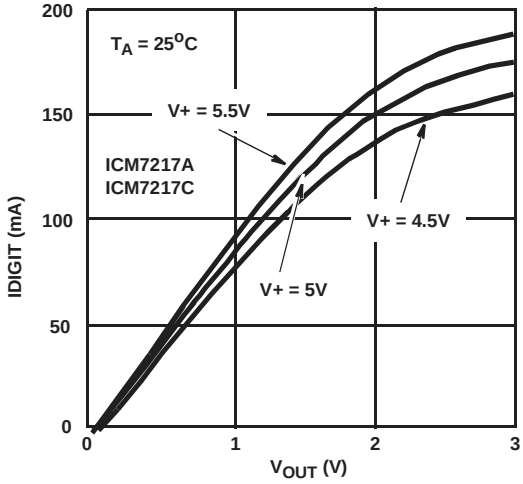


FIGURE 8. TYPICAL IDIGIT vs V_{OUT}

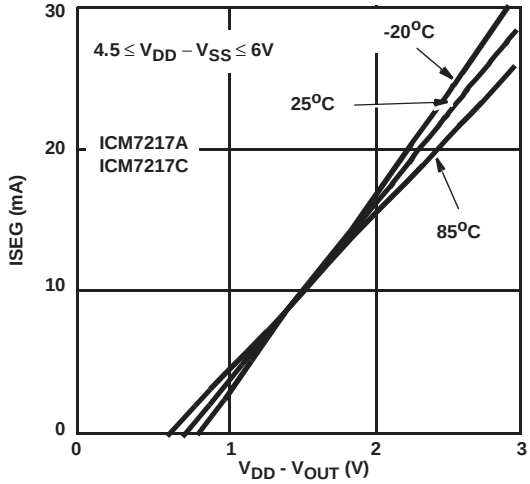


FIGURE 9. TYPICAL ISEG vs V_{DD} - V_{OUT}

Detailed Description

Control Outputs

The CARRY/BORROW output is a positive going pulse occurring typically 500ns after the positive going edge of the COUNT INPUT. It occurs when the counter is clocked from 9999 to 0000 when counting up and from 0000 to 9999 when counting down. This output allows direct cascading of counters. The CARRY/BORROW output is not valid during load counter and reset operation. When the count is 6000 or higher, a reset generates a CARRY/BORROW pulse.

The $\overline{\text{EQUAL}}$ output assumes a negative level when the contents of the counter and register are equal.

The $\overline{\text{ZERO}}$ output assumes a negative level when the content of the counter is 0000.

The CARRY/BORROW, $\overline{\text{EQUAL}}$ and $\overline{\text{ZERO}}$ outputs will drive a single TTL load over the full range of supply voltage and ambient temperature; for a logic zero, these outputs will sink 1.6mA at 0.4V and for a logic one, the outputs will source >60µA. A 10kΩ pull-up resistor to V_{DD} on the $\overline{\text{EQUAL}}$ or $\overline{\text{ZERO}}$ outputs is recommended for highest speed operation, and on the CARRY/BORROW output when it is being used for cascading. Figure 2 shows control outputs timing diagram.

Display Outputs and Control

The Digit and SEGment drivers provide a decoded 7-segment display system, capable of directly driving common anode LED displays at typical peak currents of 35mA/seg. This corresponds to average currents of 8mA/seg at 25% multiplex duty cycle. For the common cathode versions, peak segment currents are 12.5mA, corre-

sponding to average segment currents of 3.1mA. Figure 1 shows the multiplex timing. The DISPLAY pin controls the display output using three level logic. The pin is self-biased to a voltage approximately $^1/_2$ (V_{DD}); this corresponds to normal operation. When this pin is connected to V_{DD}, the segments are disabled and when connected to V_{SS}, the leading zero blanking feature is inhibited. For normal operation (display on with leading zero blanking) the pin should be left open. The display may be controlled with a 3 position SPDT switch; see Test Circuit.

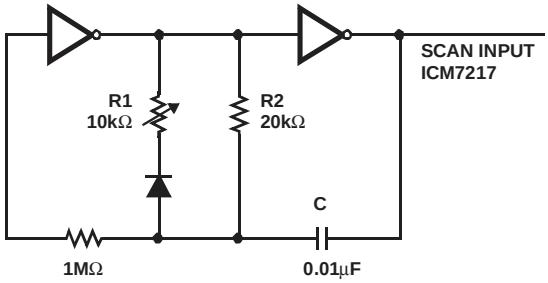


FIGURE 10A.

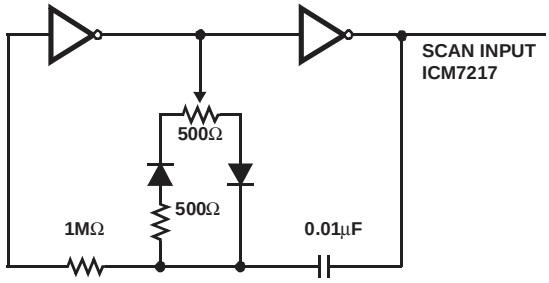


FIGURE 10B.

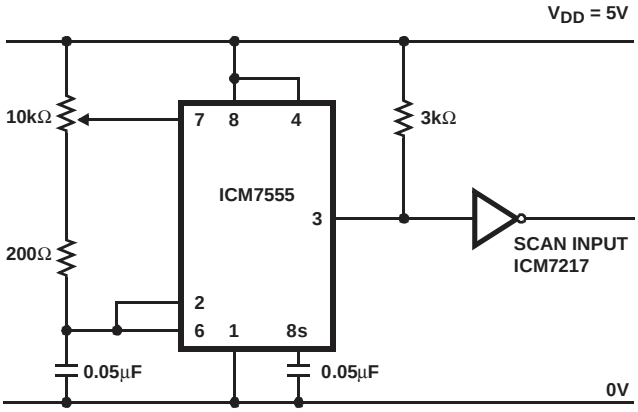


FIGURE 10C.

FIGURE 10. BRIGHTNESS CONTROL CIRCUITS

TABLE 1. ICM7217 MULTIPLEXED RATE CONTROL

SCAN CAPACITOR	NOMINAL OSCILLATOR FREQUENCY	DIGIT REPETITION RATE	SCAN CYCLE TIME (4 DIGITS)
None	2.5kHz	625Hz	1.6ms
20pF	1.25kHz	300Hz	3.2ms
90pF	600Hz	150Hz	8ms

The internal oscillator output has a duty cycle of approximately 25:1, providing a short pulse occurring at the oscillator frequency. This pulse clocks the four-state counter which provides the four multiplex phases. The short pulse width is used to delay the digit driver outputs, thereby providing inter-digit blanking which prevents ghosting. The digits are scanned from MSD (D4) to LSD (D1). See Figure 1 for the display digit multiplex timing.

Multiplex SCAN Oscillator

The on-board multiplex scan oscillator has a nominal free-running frequency of 2.5kHz. This may be reduced by the addition of a single capacitor between the SCAN pin and the positive supply. Capacitor values and corresponding nominal oscillator frequencies, digit repetition rates, and loading times are shown in Table 1.

During load counter and load register operations, the multiplex oscillator is disconnected from the SCAN input and is allowed to free-run. In all other conditions, the oscillator may be directly overdriven to about 20kHz, however the external oscillator signal should have the same duty cycle as the internal signal, since the digits are blanked during the time the external signal is at a positive level (see Figure 1). To insure proper leading zero blanking, the interdigit blanking time should not be less than about 2μs. Overdriving the oscillator at less than 200Hz may cause display flickering.

The display brightness may be altered by varying the duty cycle. Figure 10 shows several variable-duty-cycle oscillators suitable for brightness control at the ICM7217 SCAN input. The inverters should be CMOS CD4000 series and the diodes may be any inexpensive device such as IN914.

Counting Control, $\overline{\text{STORE}}$, $\overline{\text{RESET}}$

As shown in Figure 2, the counter is incremented by the

rising edge of the COUNT INPUT signal when UP/$\overline{\text{DOWN}}$ is high. It is decremented when UP/$\overline{\text{DOWN}}$ is low. A Schmitt trigger on the COUNT INPUT provides hysteresis to prevent double triggering on slow rising edges and permits operation in noisy environments. The COUNT INPUT is inhibited during reset and load counter operations.

The $\overline{\text{STORE}}$ pin controls the internal latches and consequently the signals appearing at the 7-Segment and BCD outputs. Bringing the $\overline{\text{STORE}}$ pin low transfers the contents of the counter into the latches.

The counter is asynchronously reset to 0000 by bringing the $\overline{\text{RESET}}$ pin low. The circuit performs the reset operation by forcing the BCD input lines to zero, and "presetting" all four decades of counter in parallel. This affects register loading; if LOAD REGISTER is activated when the $\overline{\text{RESET}}$ input is low, the register will also be set to zero. The $\overline{\text{STORE}}$, $\overline{\text{RESET}}$ and UP/$\overline{\text{DOWN}}$ pins are provided with pullup resistors of approximately 75kΩ.

BCD I/O Pins

The BCD I/O port provides a means of transferring data to and from the device. The ICM7217 versions can multiplex data into the counter or register via thumbwheel switches, depending on inputs to the LOAD COUNTER or LOAD REGISTER pins; (see below). When functioning as outputs, the BCD I/O pins will drive one standard TTL load. Common anode versions have internal pull down resistors and common cathode versions have internal pull up resistors on the four BCD I/O lines when used as inputs.

LOADing the COUNTER and REGISTER

The BCD I/O pins, the LOAD COUNTER (LC), and LOAD REGISTER (LR) pins combine to provide presetting and compare functions. LC and LR are 3-level inputs, being self-biased at approximately $^1/_2V_{DD}$ for normal operation. With both LC and LR open, the BCD I/O pins provide a multiplexed BCD output of the latch contents, scanned from MSD to LSD by the display multiplex.

When either the LOAD COUNTER (Pin 12) or LOAD REGISTER (Pin 11) is taken low, the drivers are turned off and the BCD pins become high-impedance inputs. When LC is connected to V_{DD}, the count input is inhibited and the levels at the BCD pins are multiplexed into the counter. When LR is connected to V_{DD}, the levels at the BCD pins are multiplexed into the register without disturbing the counter. When both are connected to V_{DD}, the count is inhibited and both register and counter will be loaded.

The LOAD COUNTER and LOAD REGISTER inputs are edge-triggered, and pulsing them high for 500ns at room temperature will initiate a full sequence of data entry cycle operations (see Figure 3). When the circuit recognizes that either or both of the LC or LR pins input is high, the multiplex oscillator and counter are reset (to D4). The internal oscillator is then disconnected from the SCAN pin and the preset circuitry is enabled. The oscillator starts and runs with a frequency determined by its internal capacitor, (which may vary from chip to chip). When the chip finishes a full 4-digit multiplex cycle (loading each digit from D4 to D3 to D2 to D1 in turn), it again samples the LOAD REGISTER and LOAD COUNTER inputs. If either or both is still high, it repeats the load cycle, if both are floating or low, the oscillator is reconnected to the SCAN pin and the chip returns to normal operation. Total load time is digit "on" time multiplied by 4. If the Digit outputs are used to strobe the BCD data into the BCD I/O inputs, the input must be synchronized to the appropriate digit (Figure 3). Input data must be valid at the trailing edge of the digit output.

When LR is connected to GROUND, the oscillator is inhibited, the BCD I/O pins go to the high impedance state, and the segment and digit drivers are turned off. This allows the display to be used for other purposes and minimizes power consumption. In this display off condition, the circuit will continue to count, and the CARRY/BORROW, $\overline{\text{EQUAL}}$, $\overline{\text{ZERO}}$, UP/$\overline{\text{DOWN}}$, $\overline{\text{RESET}}$ and $\overline{\text{STORE}}$ functions operate as normal. When LC is connected to ground, the BCD I/O pins are forced to the high impedance state without disturbing the counter or register. See "Control Input Definitions" (Table 2) for a list of the pins that function as three-state self-biased inputs and their respective operations.

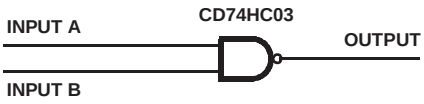
Note that the ICM7217 and ICM7217B have been designed to drive common anode displays. The BCD inputs are high true, as are the BCD outputs.

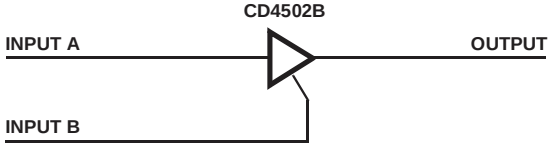
INPUT	OUTPUT
High	High
Low	Disconnected

FIGURE 11A. CMOS INVERTER

INPUT	OUTPUT
High	Disconnected
Low	High

FIGURE 11B. CMOS INVERTER





INPUT	OUTPUT	
INPUT B	INPUT A	OUTPUT
High	High	Low
High	Low	Disconnected
Low	High	Disconnected
Low	Low	Disconnected

FIGURE 11C. CMOS OPEN DRAIN

INPUT	OUTPUT	
INPUT B	INPUT A	OUTPUT
High	High	Disconnected
High	Low	Disconnected
Low	High	High
Low	Low	Low

FIGURE 11D. CMOS THREE-STATE BUFFER

FIGURE 11. DRIVING 3-LEVEL INPUTS OF ICM7217

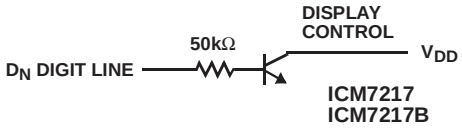


FIGURE 12A. COMMON ANODE

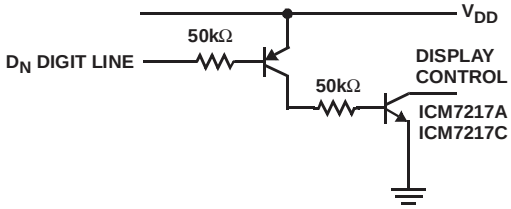


FIGURE 12B. COMMON CATHODE

FIGURE 12. FORCING LEADING ZERO DISPLAY

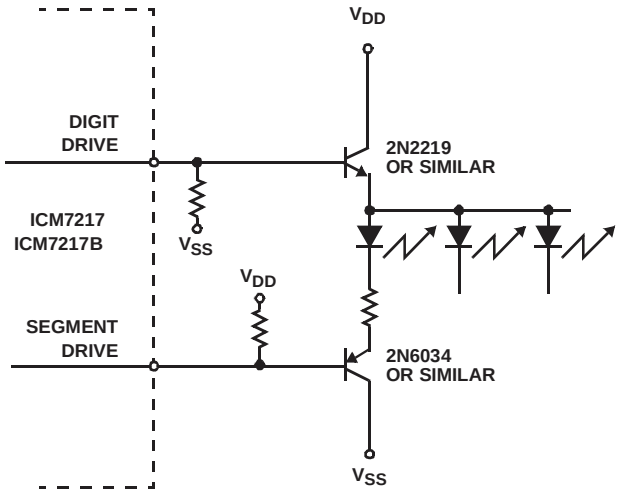


FIGURE 13A. COMMON ANODE DISPLAY

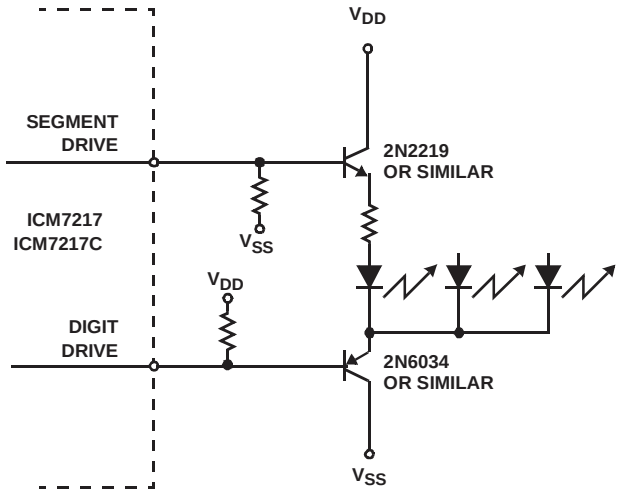


FIGURE 13B. COMMON CATHODE DISPLAY

FIGURE 13. DRIVING HIGH CURRENT DISPLAYS

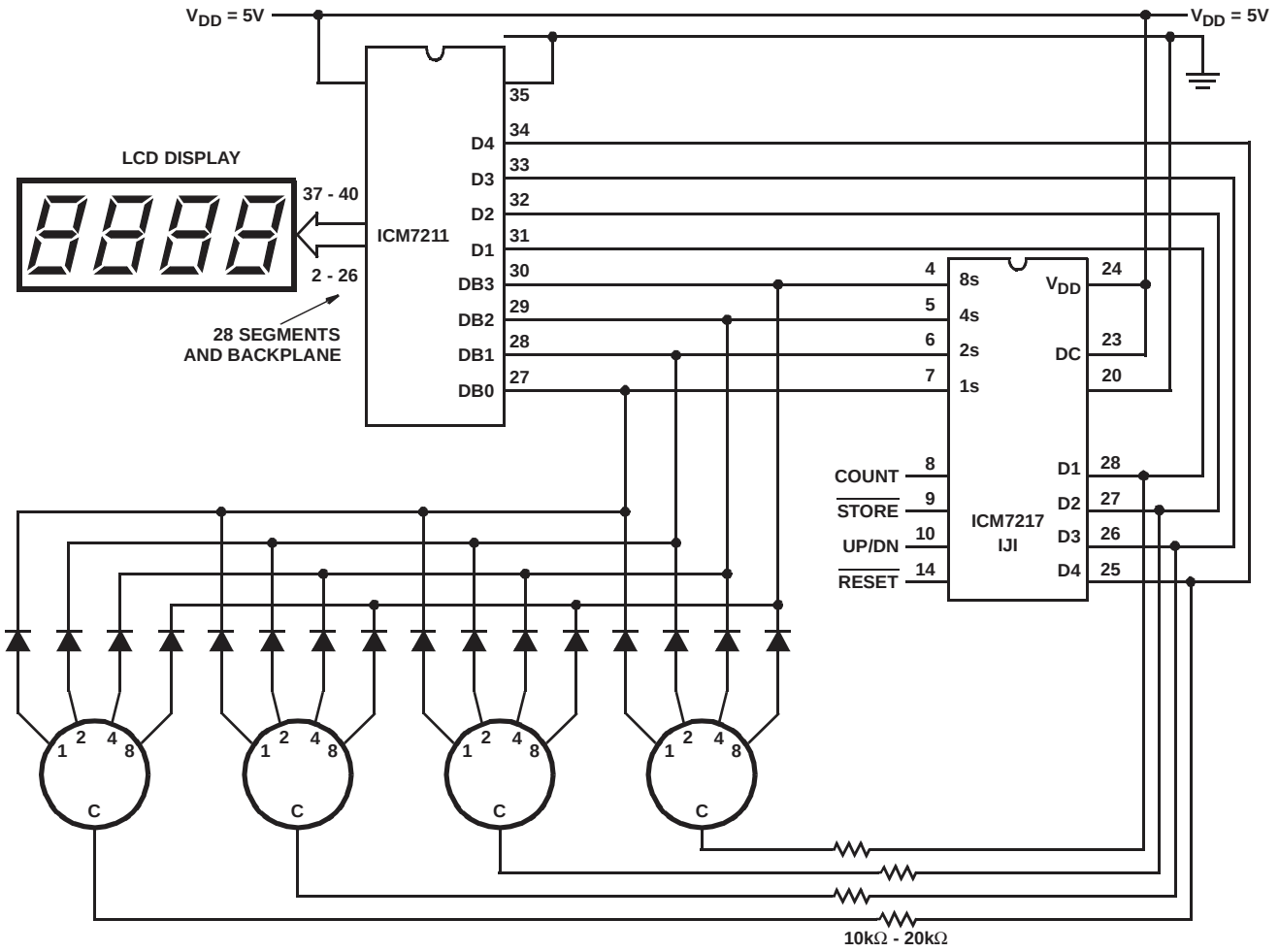


FIGURE 14. LCD DISPLAY INTERFACE (WITH THUMBWHEEL SWITCHES)

The ICM7217A and the ICM7217C are used to drive common cathode displays, and the BCD inputs are low true. BCD outputs are high true.

Notes on Thumbwheel Switches and Multiplexing

As it was mentioned, the ICM7217 is basically designed to be used with thumbwheel switches for loading the data to the device. See Figure 14 and Figure 17.

The thumbwheel switches used with these circuits (both common anode and common cathode) are TRUE BCD coded; i.e. all switches open corresponds to 0000. Since the thumbwheel switches are connected in parallel, diodes must be provided to prevent crosstalk between digits. In order to maintain reasonable noise margins, these diodes should be specified with low forward voltage drops (IN914). Similarly, if the BCD outputs are to be used, resistors should be inserted in the Digit lines to avoid loading problems.

Output and Input Restrictions

LOAD COUNTER and LOAD REGISTER operations take 1.6ms typical (5ms maximum) after LC or LR are released. During this load period the $\overline{\text{EQUAL}}$ and $\overline{\text{ZERO}}$ outputs are not valid (see Figure 3). Since the Counter and register are compared by XOR gates, loading the counter or register can cause erroneous glitches on the $\overline{\text{EQUAL}}$ and $\overline{\text{ZERO}}$ outputs when codes cross.

LOAD COUNTER or LOAD REGISTER, and $\overline{\text{RESET}}$ input can not be activated at the same time or within a short period of each other. Operation of each input must be delayed 1.6ms typical (5ms for guaranteed proper operation) relating to the preceding one.

Counter and register can be loaded together with the same value if LC and LR inputs become activated exactly at the same time.

Notice the setup and hold time of UP/DOWN input when it is changing during counting operation. Violation of UP/ $\overline{\text{DOWN}}$ hold time will result in incrementing or decrementing the counter by 1000, 100 or 10 where the preceding digit is transitioning from 5 to 6 or 6 to 5.

The $\overline{\text{RESET}}$ input may be susceptible to noise if its input rise time is greater than about 500µs This will present no problems when this input is driven by active devices (i.e., TTL or CMOS logic) but in hardwired systems adding virtually any capacitance to the $\overline{\text{RESET}}$ input can cause trouble. A simple circuit which provides a reliable power-up reset and a fast rise time on the $\overline{\text{RESET}}$ input is shown on Figure 15.

When using the circuit as a programmable divider (÷ by n with equal outputs) a short time delay (about 1µs) is needed from the $\overline{\text{EQUAL}}$ output to the $\overline{\text{RESET}}$ input to establish a pulse of adequate duration. (See Figure 16).

When the circuit is configured to reload the counter or register with a new value from the BCD lines (upon reaching $\overline{\text{EQUAL}}$), loading time will be digit "on" time multiplied by four. If this load time is longer than one period of the input count, a count can be lost. Since the circuit will retain data in the register, the register need only be updated when a new value is to be entered. $\overline{\text{RESET}}$ will not clear the register.

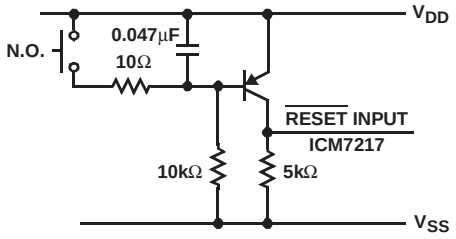


FIGURE 15. POWER ON RESET

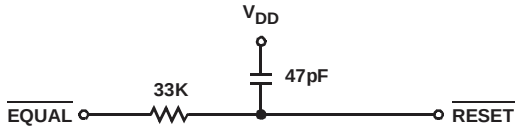
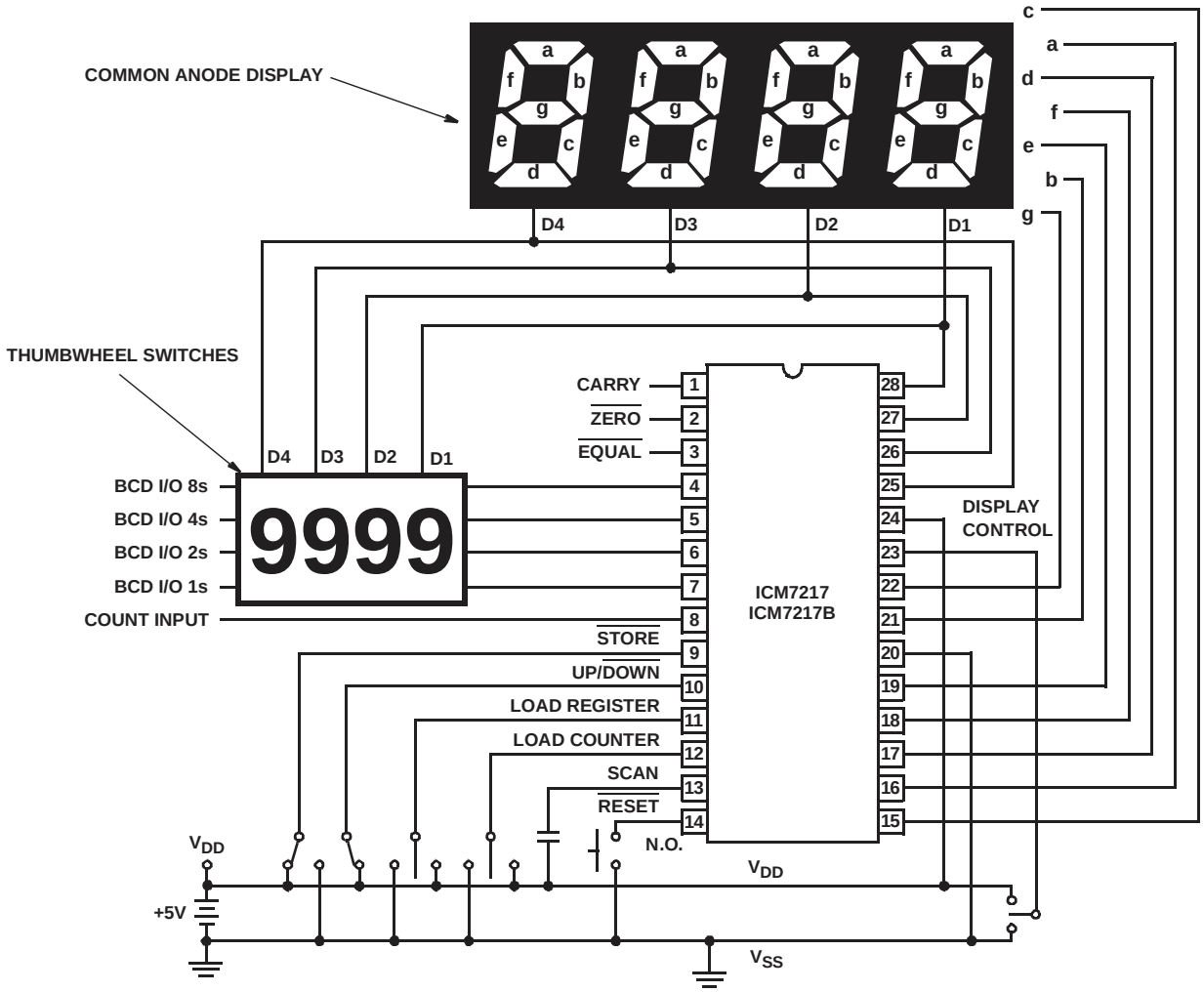


FIGURE 16. $\overline{\text{EQUAL}}$ TO $\overline{\text{RESET}}$ DELAY

Test Circuit



Applications

3-Level Inputs

ICM7217 has three inputs with 3-level logic states; High, Low and Disconnected. These inputs are: LOAD REGISTER/OFF, LOAD COUNTER/I/O OFF and DISPLAY CONT.

The circuits illustrated on Figure 11 can be used to drive these inputs in different applications.

Fixed Decimal Point

In the common anode versions, a fixed decimal point may be activated by connecting the DP segment lead from the appropriate digit (with separate digit displays) through a 39Ω series resistor to Ground. With common cathode devices, the DP segment lead should be connected through a 75Ω series resistor to V_{DD}.

To force the device to display leading zeroes after a fixed decimal point, use a bipolar transistor and base resistor in a configuration like that shown in Figure 12 with the resistor connected to the digit output driving the DP for left hand DP displays, and to the next least significant digit output for right hand DP display.

Driving Larger Displays

For displays requiring more current than the ICM7217 can provide, the circuits of Figure 13 can be used.

LCD Display Interface

The low-power operation of the ICM7217 makes an LCD interface desirable. The Intersil ICM7211 4-digit, BCD-to-LCD display driver easily interfaces to the ICM7217 as shown in Figure 14. Total system power consumption is less than 5mW. System timing margins can be improved by using capacitance to ground to slow down the BCD lines.

The 10kΩ - 20kΩ resistors on the switch BCD lines serve to isolate the switches during BCD output.

Unit Counter with BCD Output

The simplest application of the ICM7217 is a 4-digit unit counter (Figure 18). All that is required is an ICM7217, a power supply and a 4 digit display. Add a momentary switch for reset, an SPDT center-off switch to blank the display or view leading zeroes, and one more SPDT switch for up/down control. Using an ICM7217A with a common-cathode calculator-type display results in the least expensive digital counter/display system available.

Inexpensive Frequency Counter/ Tachometer

This circuit uses the low power ICM7555 (CMOS 555) to generate the gating, STORE and RESET signals as shown in Figure 19. To provide the gating signal, the timer is configured as an a stable multivibrator, using R_A, R_B and C to provide an output that is positive for approximately one second and negative for approximately 300µs - 500µs. The positive waveform time is given by $t_{WP} = 0.693 (R_A + R_B)C$ while the negative waveform is given by two = $0.693 R_BC$. The system is calibrated by using a 5MΩ potentiometer for R_A as a “coarse” control and a 1kΩ potentiometer for R_B as a “fine” control. CD40106Bs are used as a monostable multivibrator and reset time delay.

Tape Recorder Position Indicator/controller

The circuit in Figure 20 shows an application which uses the up/down counting feature of the ICM7217 to keep track of tape position. This circuit is representative of the many applications of up/down counting in monitoring dimensional position.

In the tape recorder application, the LOAD REGISTER, EQUAL and ZERO outputs are used to control the recorder. To make the recorder stop at a particular point on the tape, the register can be set with the stop point and the EQUAL output used to stop the recorder either on fast forward, play or rewind.

To make the recorder stop before the tape comes free of the reel on rewind, a leader should be used. Resetting the counter at the starting point of the tape, a few feet from the end of the leader, allows the ZERO output to be used to stop the recorder on rewind, leaving the leader on the reel.

The 1MΩ resistor and 0.0047µF capacitor on the COUNT INPUT provide a time constant of about 5ms to debounce the reel switch. The Schmitt trigger on the COUNT INPUT of the ICM7217 squares up the signal before applying it to the counter. This technique may be used to debounce switch-closure inputs in other applications.

Precision Elapsed Time/Countdown Timer

The circuit in Figure 21 uses an ICM7213 precision one minute/one second timebase generator using a 4.1943MHz crystal for generating pulses counted by an ICM7217B. The thumbwheel switches allow a starting time to be entered into the counter for a preset-countdown type timer, and allow the register to be set for compare functions. For instance, to make a 24-hour clock with BCD output the register can be preset with 2400 and the EQUAL output used to reset the counter. Note the 10K resistor connected between the LOAD COUNTER terminal and Ground. This resistor pulls the LOAD COUNTER input low when not loading, thereby inhibiting the BCD output drivers. This resistor should be eliminated and SW4 replaced with an SPDT center-off switch if the BCD outputs are to be used.

This technique may be used on any 3-level input. The 100kΩ pullup resistor on the count input is used to ensure proper logic voltage swing from the ICM7213. For a less expensive (and less accurate) timebase, an ICM7555 timer may be used in a configuration like that shown in Figure 19 to generate a 1Hz reference.

8-Digit Up/Down Counter

This circuit (Figure 22) shows how to cascade counters and retain correct leading zero blanking. The NAND gate detects whether a digit is active since one of the two segments $\overline{a}$ or $\overline{b}$ is active on any unblanked number. The flip flop is clocked by the least significant digit of the high order counter, and if this digit is not blanked, the Q output of the flip flop goes high and turns on the NPN transistor, thereby inhibiting leading zero blanking on the low order counter.

It is possible to use separate thumbwheel switches for presetting, but since the devices load data with the oscillator free-running, the multiplexing of the two devices is difficult to synchronize.

Precision Frequency Counter/Tachometer

The circuit shown in Figure 23 is a simple implementation of a four digit frequency counter, using an ICM7207A to provide the one second gating window and the STORE and RESET signals. In this configuration, the display reads hertz directly. With Pin 11 of the ICM7027A connected to V_{DD}, the gating time will be 0.1s; this will display tens of hertz at the least significant digit. For shorter gating times, an ICM7207 may be used (with a 6.5536MHz crystal), giving a 0.01s gating with Pin 11 connected to V_{DD}, and a 0.1s gating with Pin 11 open.

To implement a four digit tachometer, the ICM7207A with one second gating should be used. To get the display to read directly in RPM, the rotational frequency of the object to be measured must be multiplied by 60. This can be done electronically using a phase-locked loop, or mechanically by using a disc rotating with the object with the appropriate number of holes drilled around its edge to interrupt the light from an LED to a photo-dector. For faster updating, use 0.1s gating, and multiply the rotational frequency by 600.

Auto-Tare System

This circuit uses the count-up and count-down functions of the ICM7217, controlled via the EQUAL and ZERO outputs, to count in SYNC with an ICL7109A and ICL7109D Converter as shown in Figure 24. By RESETing the ICM7217 on a “tare” value conversion, and STORE-ing the result of a true value conversion, an automatic fare subtraction occurs in the result.

The ICM7217 stays in step with the ICL7109 by counting up and down between 0 and 4095, for 8192 total counts, the same number as the ICL7109 cycle. See applications note No. A047 for more details.

TABLE 2. CONTROL INPUT DEFINITIONS ICM7217

INPUT	TERMINAL	VOLTAGE	FUNCTION
STORE	9	V_{DD} (or floating) V_{SS}	Output Latches Not Updated Output Latches Updated
UP/$\overline{\text{DOWN}}$	10	V_{DD} (or floating) V_{SS}	Counter Counts Up Counter Counts Down
$\overline{\text{RESET}}$	14	V_{DD} (or floating) V_{SS}	Normal Operation Counter Reset
LOAD COUNTER/ $\overline{\text{I/O OFF}}$	12	Unconnected V_{DD} V_{SS}	Normal Operation Counter Loaded with BCD data BCD Port Forced to Hi-Z Condition
LOAD REGISTER/ $\overline{\text{OFF}}$	11	Unconnected V_{DD} V_{SS}	Normal Operation Register Loaded with BCD Data Display Drivers Disabled; BCD Port Forced to Hi-Z Condition, mpx Counter Reset to D4; mpx Oscillator Inhibited
DISPLAY CONTrol	23 Common Anode 20 Common Cathode	Unconnected V_{DD} V_{SS}	Normal Operation Segment Drivers Disabled Leading Zero Blanking Inhibited

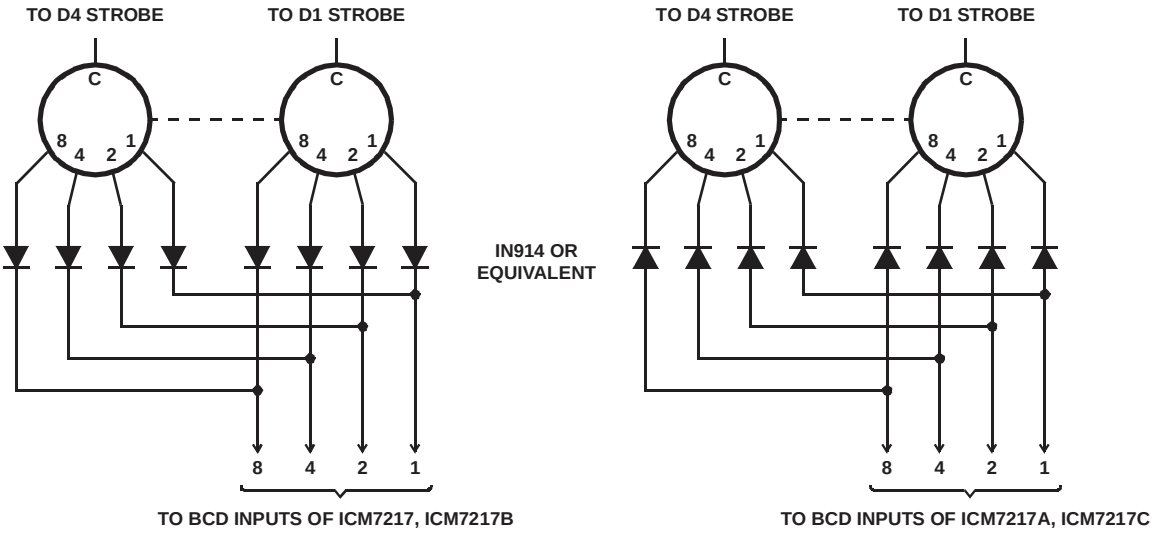


FIGURE 17. THUMBWHEEL SWITCH/DIODE CONNECTIONS

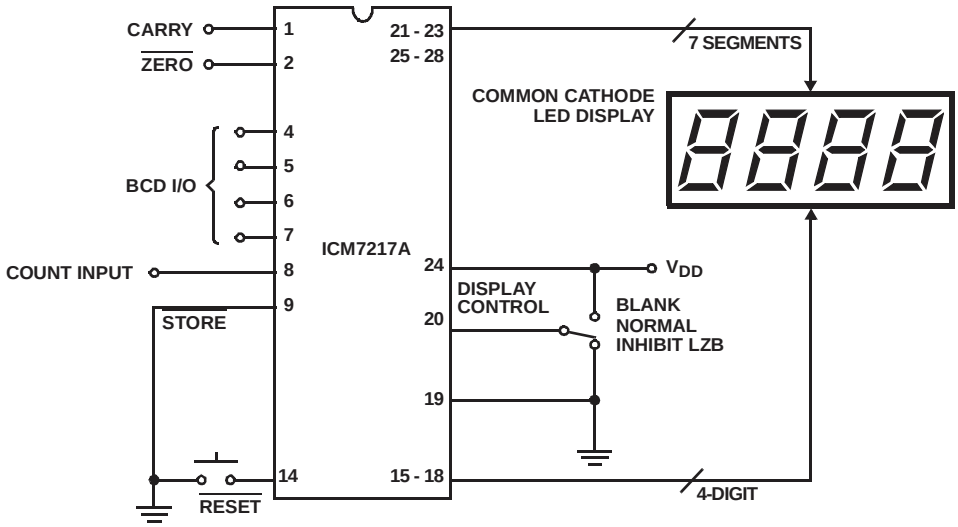


FIGURE 18. UNIT COUNTER

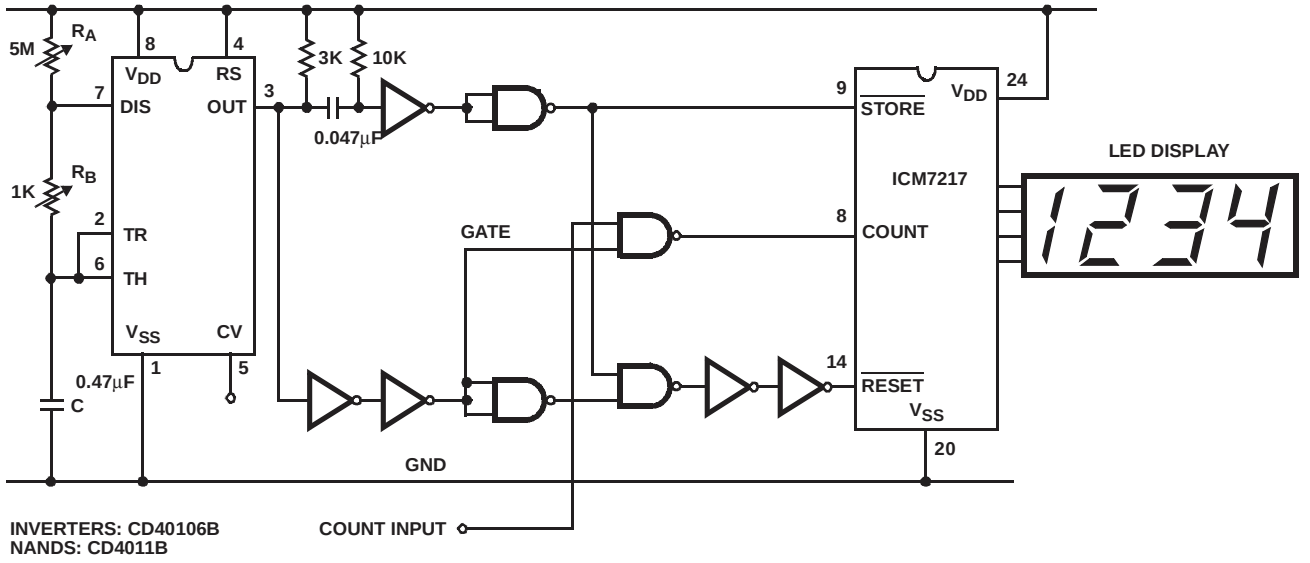


FIGURE 19A.

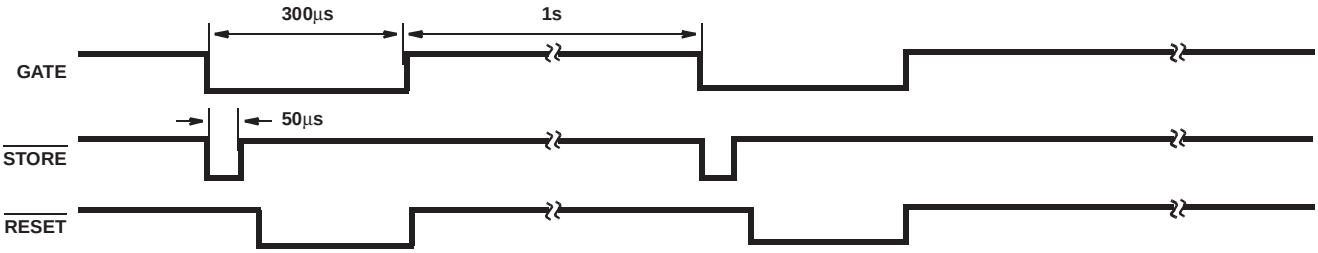


FIGURE 19B.

FIGURE 19. INEXPENSIVE FREQUENCY COUNTER

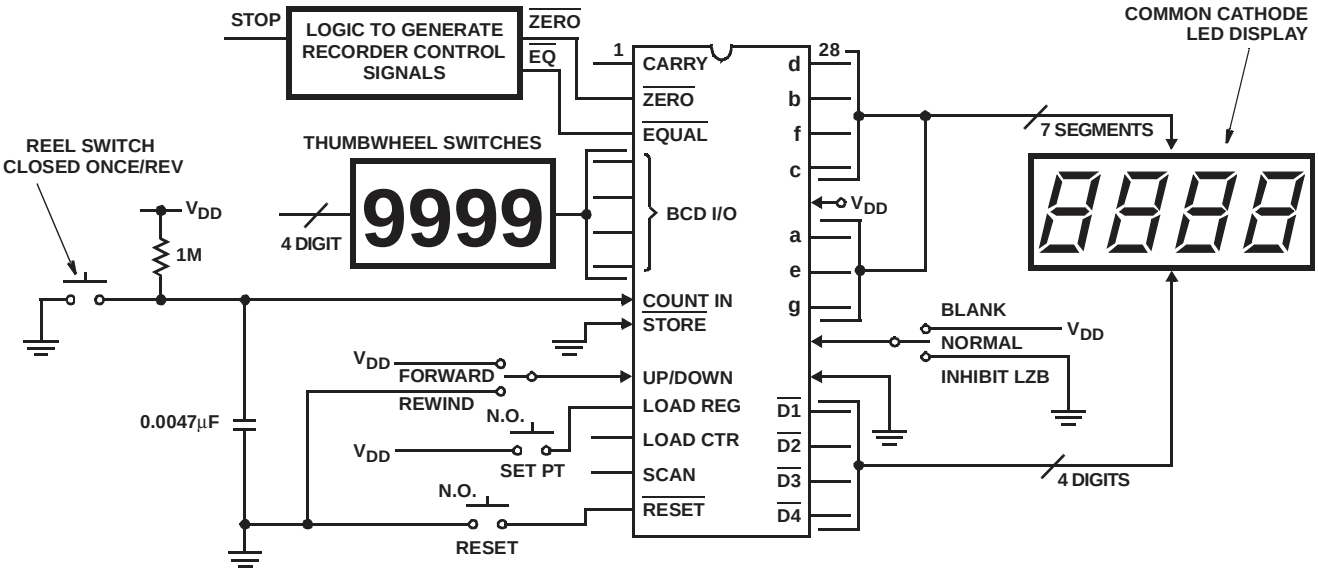


FIGURE 20. TAPE RECORDER POSITION INDICATOR

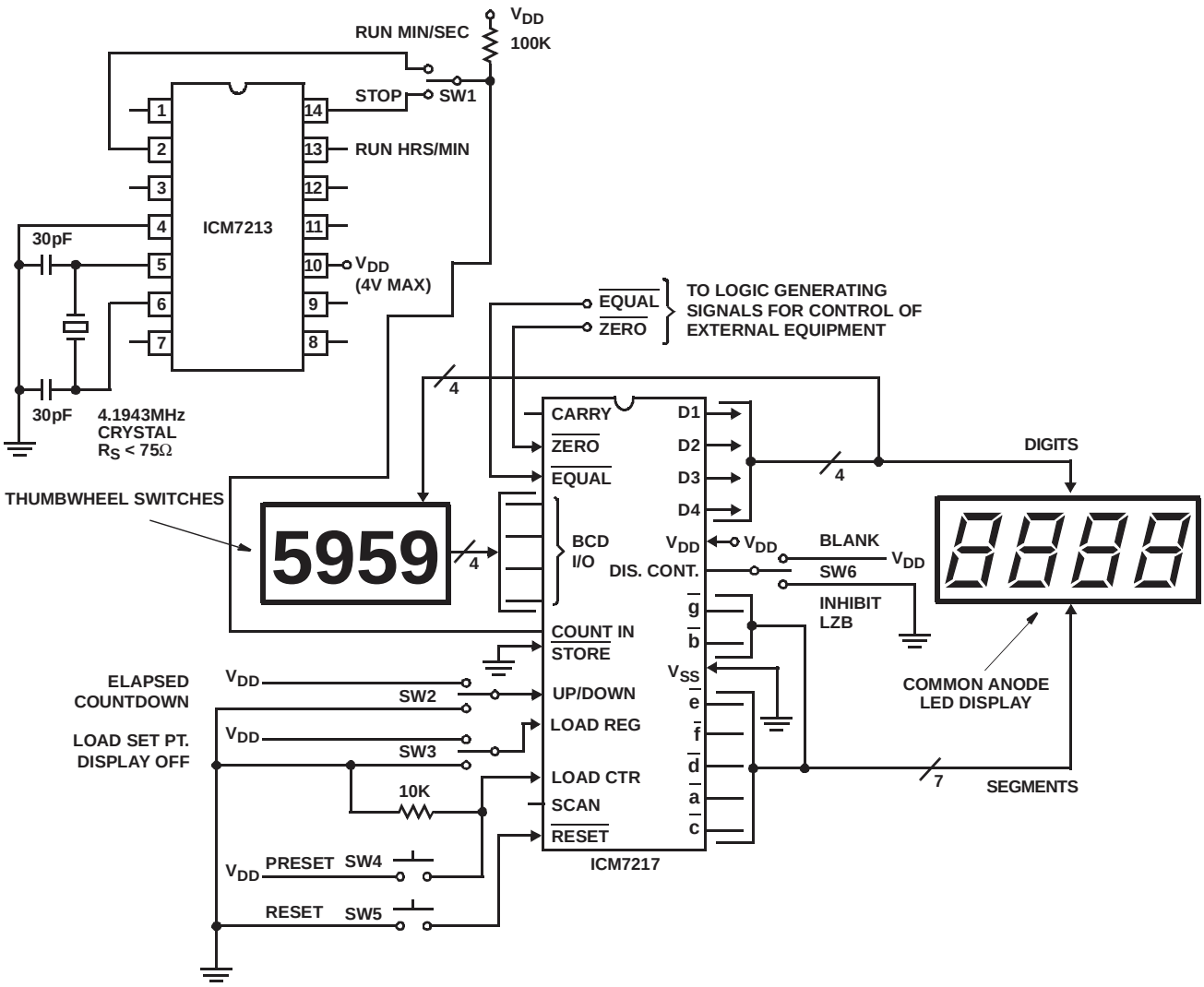


FIGURE 21. PRECISION TIMER

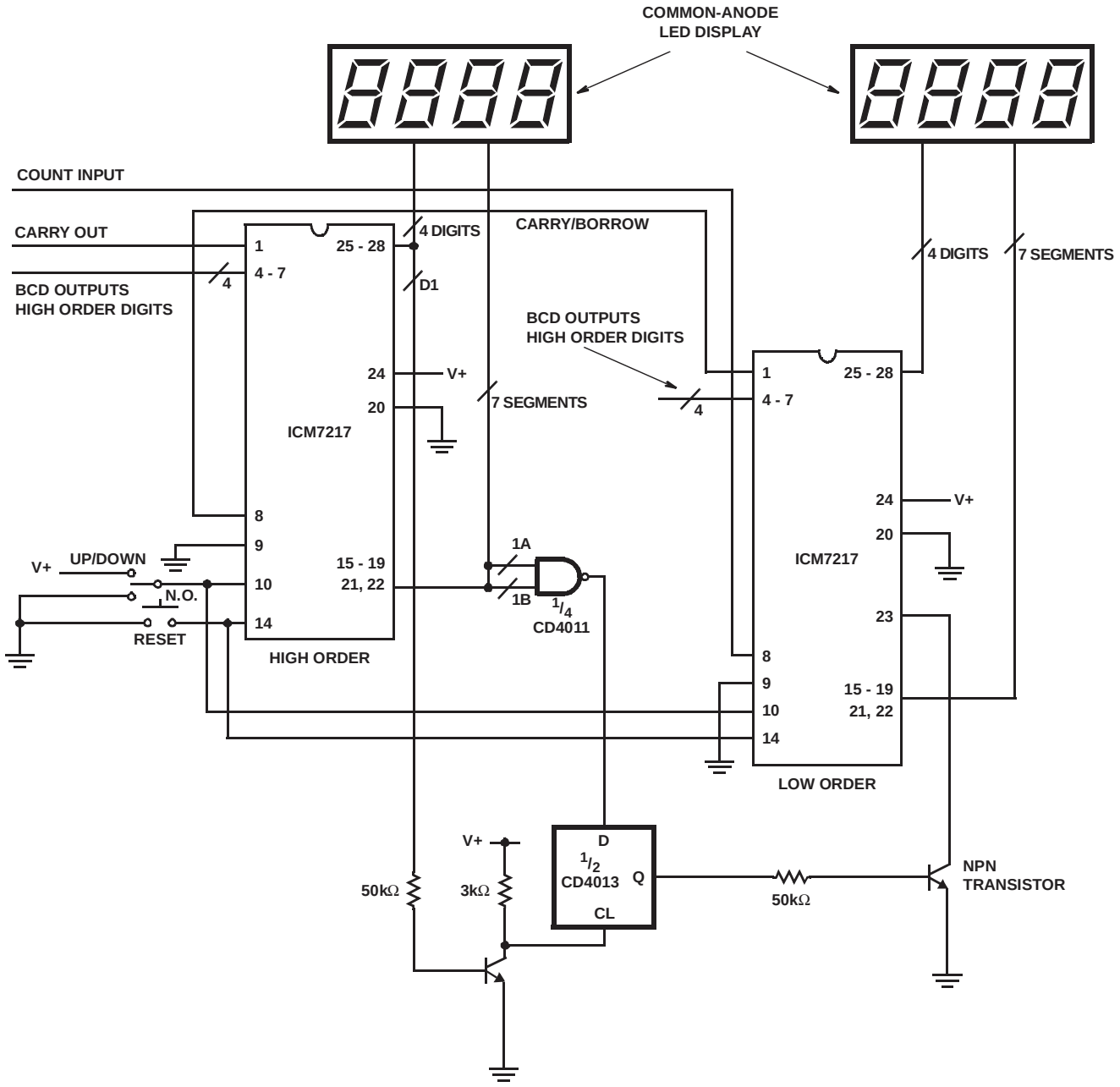


FIGURE 22. 8-DIGIT UP/DOWN COUNTER

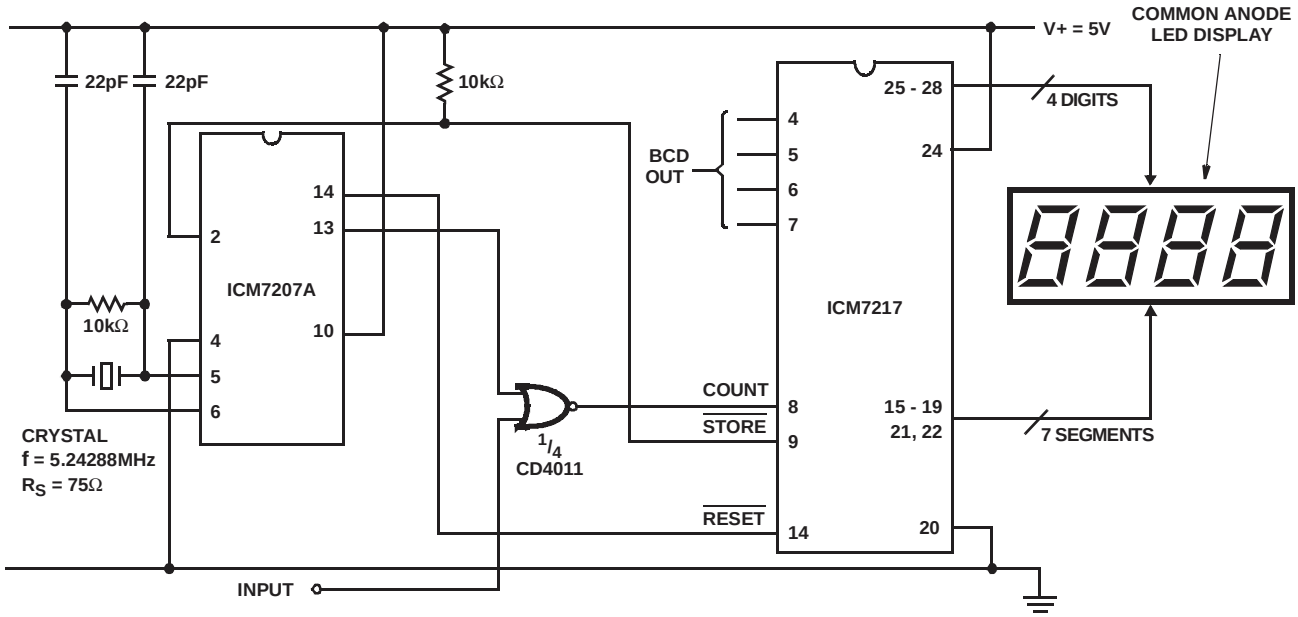


FIGURE 23. PRECISION FREQUENCY COUNTER (MHz MAXIMUM)

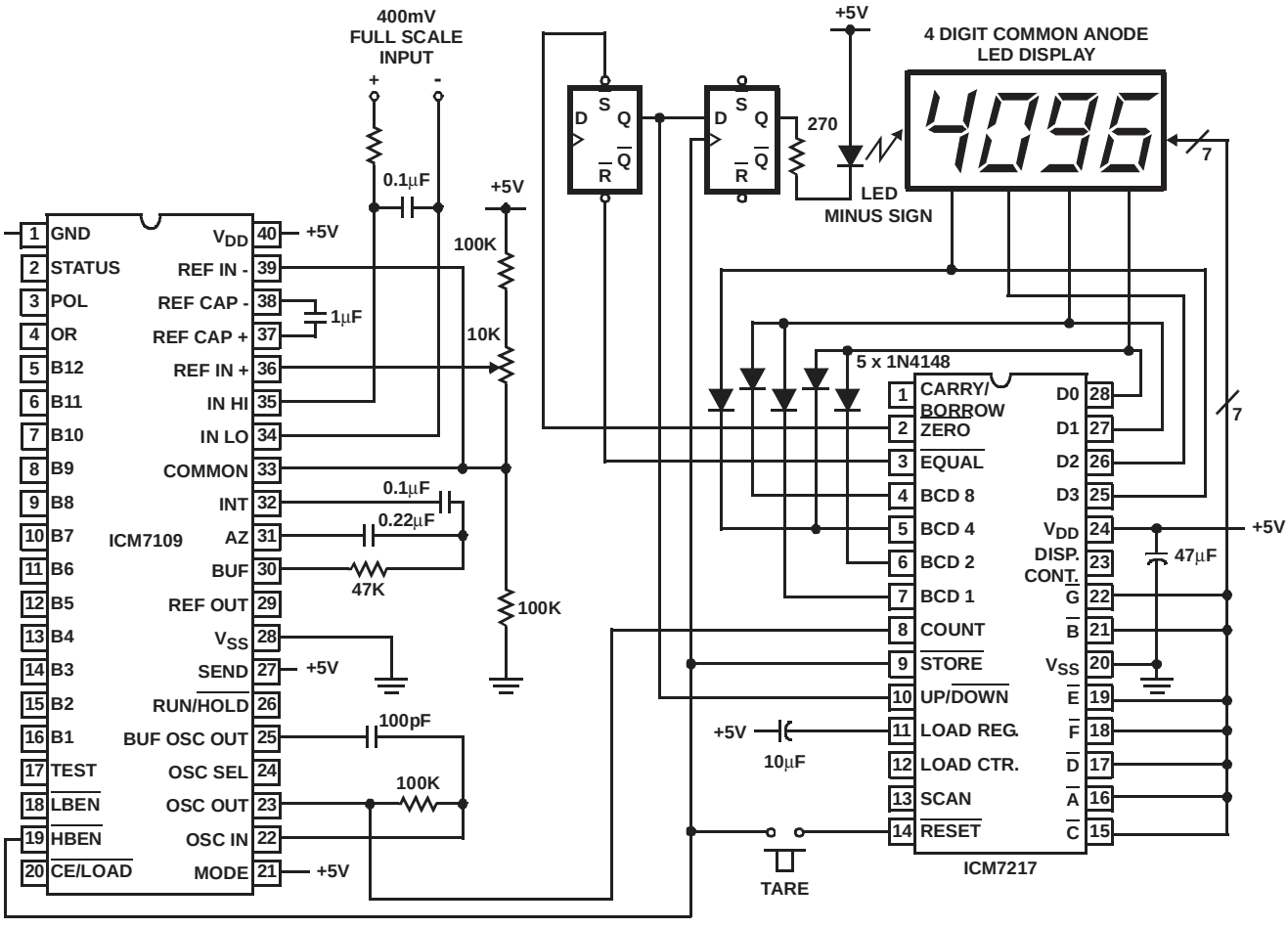


FIGURE 24. AUTO-TARE SYSTEM FOR A/D CONVERTER

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